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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,056	ASAYAMA ET AL.	
	Examiner	Art Unit	
	Evan Pert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31,32 and 36-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *50-55* is/are allowed.

6)☒ Claim(s) *31,32,36-49 and 56-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. 6,159,826).

Regarding claim 31, Kim et al. disclose a method for manufacturing a semiconductor device comprising forming 1st electrode pads (56b) comprised of an uppermost wiring layer (56) in a scribe region (34) and a bonding pad (56a) comprised of the uppermost wiring in a product circuit region (32); forming a protection film (57) on an upper layer of said uppermost layer wiring (56); and partially exposing a surface of said bonding pad by removing a predetermined part of said protection film (i.e. openings selectively formed at 56a and 56b).

Regarding claim 32, Kim et al. disclose forming second electrode pads and comprised of said uppermost layer wiring (56) and the partially exposing step of the 1st pad includes partially exposing a surface of the second pad (i.e. both opening are formed to expose pads in and out of the scribe region).

Kim et al. are silent about dimensions of the electrode probing and bonding pads provided in their invention. Yet, the examiner takes Official Notice that a plethora of references are available that disclose the advantageous trend of miniaturization in semiconductor devices, including shrinking pad sizes.

Furthermore, the courts have ruled that a size limitation is not novel over the prior art unless an unexpected result is achieved **[MPEP 2144.04, Section IV A].**

In the instant case, applicant recites dimensions that include pad sizes generally smaller than discussed in the prior art, but fails to recite any unexpected result of the particularly claimed sizes

It would have been obvious to one of ordinary skill in the art to choose pad sizes in the scribe and product regions as small as possible. In so doing, one of ordinary skill would be motivated to retain a certain minimum size based on the minimum sizes of available probes and bond-wires, to thus arrive at any probing pad size and any bonding pad size, wherein a probe can make electrical contact and a bonding wire can be attached, respectively.

Kim et al. do not specifically disclose that the uppermost wiring layer is patterned by "a lithography method." Yet, the examiner takes Official Notice that creating a conductive pattern of a wafer by a lithography method has been notoriously well known for decades and is advantageous for creating a large amount of pattern in a single exposure step.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt a lithography method to pattern layer 56 in Kim et al., motivated to create many patterns simultaneously as is notoriously well known in the art.

2. Claims 36-39, 43-44, 46, and 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al., as applied to claim 31 above, and further in view of Marcus et al. (U.S. 5,475,318) taken with Sugasawara (U.S. 5,936,876).

Regarding claims 36-39, 46 and 48, Kim et al. is silent about a particular radius of curvature of probe 60 depicted contacting a 1st electrode pad in the scribe region.

Marcus et al. disclose microprobes (abstract) suitable for wafer probing (col. 7). These probes are so small that one of ordinary skill would be motivated to make probing pads on the chip very small on the order of the probe. As taught by Sugasawara, the size of probing pads is not critical, but can be made much smaller than wire bonding pads (brief summary text 16).

Furthermore, one of ordinary skill in the art would be motivated to make smaller and smaller probe pads and bond pads to increase silicon real estate [abstract], but would be motivated to place a lower bound on size on each of the probing pad and bond pad, based on the probe size and bond wire size, respectively.

Regarding claims 44 and 49, Sugasawara discloses the techniques of selective etching or FIB to expose the probing pads from underneath the protection layer [col. 7]. It would have been obvious to one of ordinary skill in the art to selectively remove the protection layer of the pads using FIB or selective etch, motivated to make electrical contact with the pad(s) as disclosed by Sugasawara.

Regarding claim 43, the pads are in a "island shape" (i.e. a rectangular island shape).

Regarding claims 45 and 47, it would have been obvious to include an additional pad in the scribe line common to a plurality of TEGs for the purposes of providing a common ground or a supply rail, for example, as is known in the art when testing at the wafer level.

Regarding claims 41 and 42, the references are silent about an overlap size of a pad as compared to the diameter of the connect hole via, a concept known in the art as "framing" the via. Again, the courts have ruled that limitations of size do not distinguish from the prior art unless an unexpected result is attained. It would have been obvious to one of ordinary skill in the art to size the pad larger than the via to assure a good electrical path from the via to the pad, in view of the well known concepts of misregistration and contact resistance.

3. Claims 56, 57, 58, 59 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al., in view of Marcus et al. (U.S. 5,475,318) with Sugasawara (U.S. 5,936,876), as applied to claims 36, 38, 39, 46, 48 above, and further in view of US 5,764,072.

Kim et al., Marcus et al. and Sugasawara are silent about "tungsten" for the "main component" of the "probes."

US 5,764,072 teaches that "preferred metal for probes are beryllium copper, ***tungsten*** or 3% rhenium tungsten because they have good resistance to oxidation, are good conductors, are resilient and springy, and have good wear properties."

It would have been obvious to one of ordinary skill in the art to adopt "tungsten" as the "main component" for any "probe" to contact a TEG pad, motivated by good resistance to oxidation, good electrical conductivity, resilience, and good wear properties, as disclosed in the '072 patent.

Response to Arguments

4. Applicant argues that the pending claims are patentable because of smaller size limitations as compared to the prior art, particularly smaller electrode pads that are touched with probe needles for testing. Yet, the ordinary of skill recognize that TEG features take up space on a semiconductor wafer placed as part of chip areas or regions in between chips (i.e. scribe lines) so there is nothing unexpected about shrinking TEG features (e.g. pads) to allow the placement of more TEGs in the same space. This is the age-old idea of miniaturization, the trend of all semiconductor devices.

Yet, applicant argues that the novelty of applicant's invention is in recognizing that smaller pad sizes for TEGs "unexpectedly" allows more data and efficiency for testing by having more TEGs in the same space.

For the reader unfamiliar with "TEG", the examiner cites, but does not rely on, U.S. 6,319,792: In col. 2, lines 6, the '792 patent discusses TEGs on a wafer and points out the obvious fact that "the pattern density of the TEG region...is under a restriction in the total size of the plurality of pads which occupy a great part of the TEG region." While the '792 patent is referring to TEG elements in a chip region, moving the elements to the scribe region was known before applicant's filing as evidenced by U.S. 6,368,943, for example, which alludes to "process monitoring called 'Scribe TEG (Test Element Group)' within the scribe line area for the purpose of shrinking the chip."

Applicant must define the claimed invention by limitations other than a smaller size because the courts have held that a change in size of the prior art is not patentable unless there is a novel and unexpected result. In the instant case, the fact that smaller TEG pads means more pads in the same space is not unexpected.

Allowable Subject Matter

5. Claims 50-55 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose the claimed method wherein a particular combination of extraction electrode pads in a scribe region and product region are provided and pads in the scribe region measured by contacting a probe with rounded tip wherein logic circuits are provided as TEG elements probed in the scribe region.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:30AM-3:30 PM). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-0956.

EVAN PERT
PRIMARY EXAMINER

ETP
November 3, 2003